Exhibit M

MacInnis 7,530,027 Applied to Representative Renesas, Panasonic, Denso Ten, and Toyota Accused Products

This claim chart compares independent claim 11 of U.S. Patent No. 7,530,027 ("the MacInnis '027 patent") to Renesas's R-Car H3 system on a chip ("SoC").

On information and belief, Renesas's R-Car H3 SoC is representative of other Renesas infotainment and high-end car information system SoCs having similar functionality ("Accused Renesas Infotainment SoCs"), including, and without limitation, the Renesas R-Car H2 and the Renesas R-Mobile A1. *See* Declaration of Dr. Joseph Havlicek ("Ex. 67, Havlicek Decl.") ¶¶ 11-13.

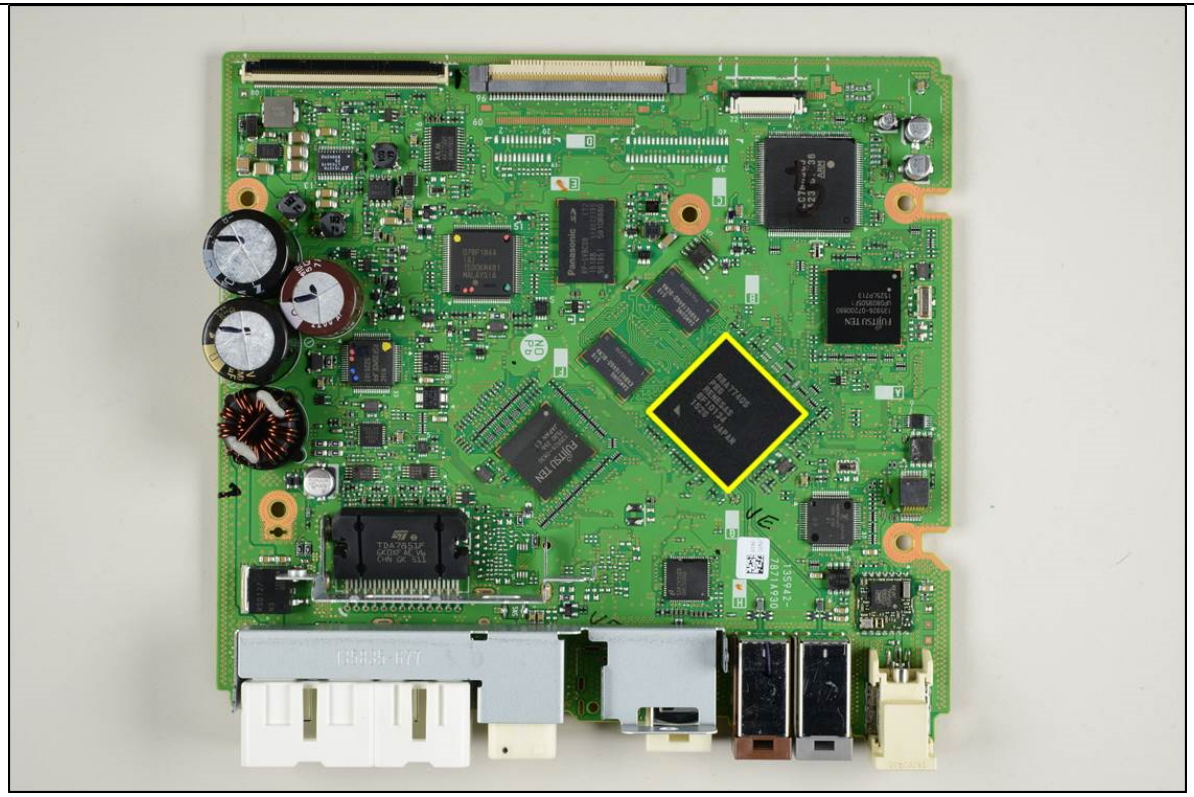
The R-Car H2 SoC is incorporated in downstream products, including without limitation, Panasonic head units, such as Ser No. 112905, that form Accused Toyota Navigation units, including Camry Navigation System with WiFi Hotspot (86840-06011).

The R-Mobile A1 SoC is incorporated in downstream products, including without limitation, at least Denso Ten, formerly Fujitsu Ten, head units, such as Ser. Nos. MMA00002, MM910406, and MM100046, which are incorporated in Accused Toyota Navigation units, including Camry Receiver (86804-06180), Corolla Nav System Kit (86804-02070), and Camry Navigation System Receiver (86804-06100).

On information and belief, the Accused Renesas Infotainment SoCs, and head units and automobiles that incorporate the Accused Renesas Infotainment SoCs, infringe directly, indirectly, and/or under the doctrine of equivalents at least claim 11 of the MacInnis '027 patent.

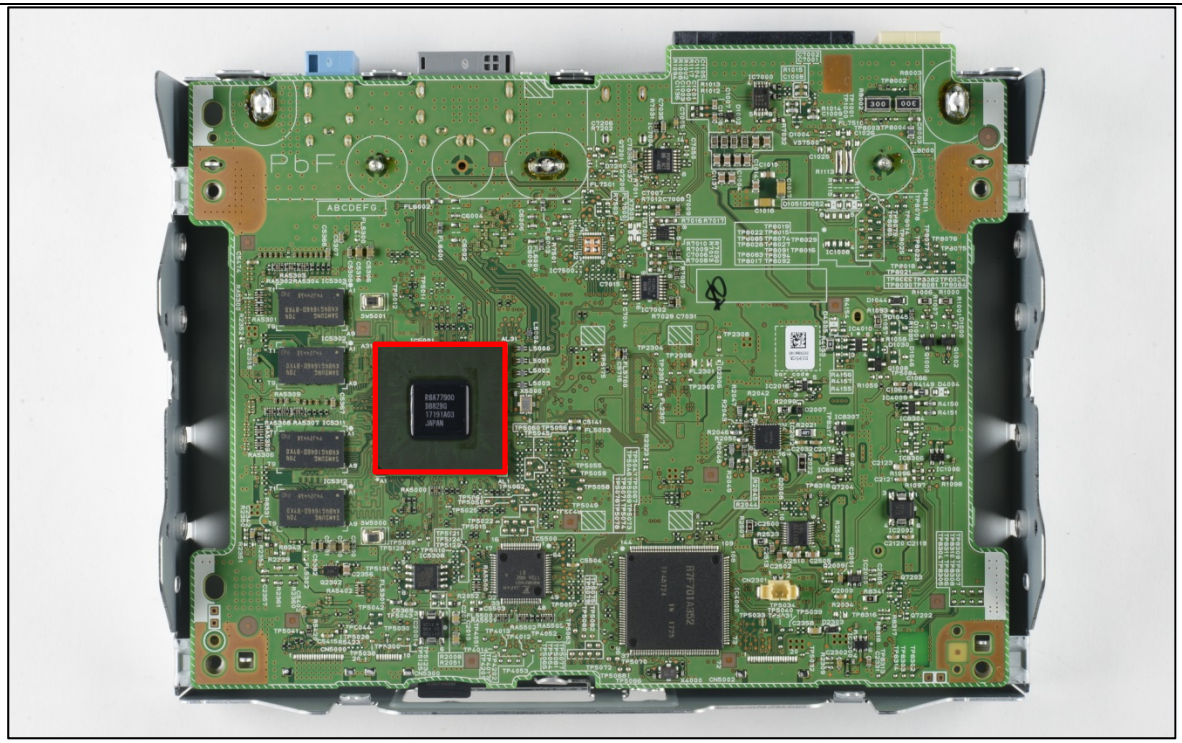
Claim – U.S. Patent No. 7,530,027 (MacInnis)	**Application of Claim Language to Accused Product**
Claim 11	
A system for processing graphics images, comprising:	To the extent that the preamble is deemed limiting, the Accused Renesas Infotainment SoCs and head units and automobiles that incorporate the Accused Renesas Infotainment SoCs comprise a system for processing graphics images. At least the Fujitsu Ten (MM910406) head unit, which is included in at least the Toyota Corolla Navigation System Kit (26187), includes a Renesas R-Mobile A1 SoC (highlighted in yellow).

	 TOYOTA 86804-02070 FUJITSU TEN 139000-0690B101 ASSEMBLED IN MEXICO S/NO. MM910406 MANUFACTURER FUJITSU TEN LIMITED ADDRESS 2-28, Gosho-dori 1-chome Hyogo-ku, Kobe 652-8510, JAPAN MANUFACTURED September 2015 Complies with 21 CFR Chapter 1, Subchapter J. This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. HD Radio Technology manufactured under license from iBiquity Digital Corporation. U.S. and Foreign Patents. HD Radio™ and the HD, HD Radio, and "Arc" logos are proprietary trademarks of iBiquity Digital Corp. AM 530 to 1710kHz FM 87.75 to 107.9MHz FCC ID: BABFT0044C IC: 2024B-FT0044C Model: FT0044C RCPFUFT12-1493 TYPE: FT0044D microSDHC Logo is a trademark of SD-3C, LLC. MM910406 86804-02070

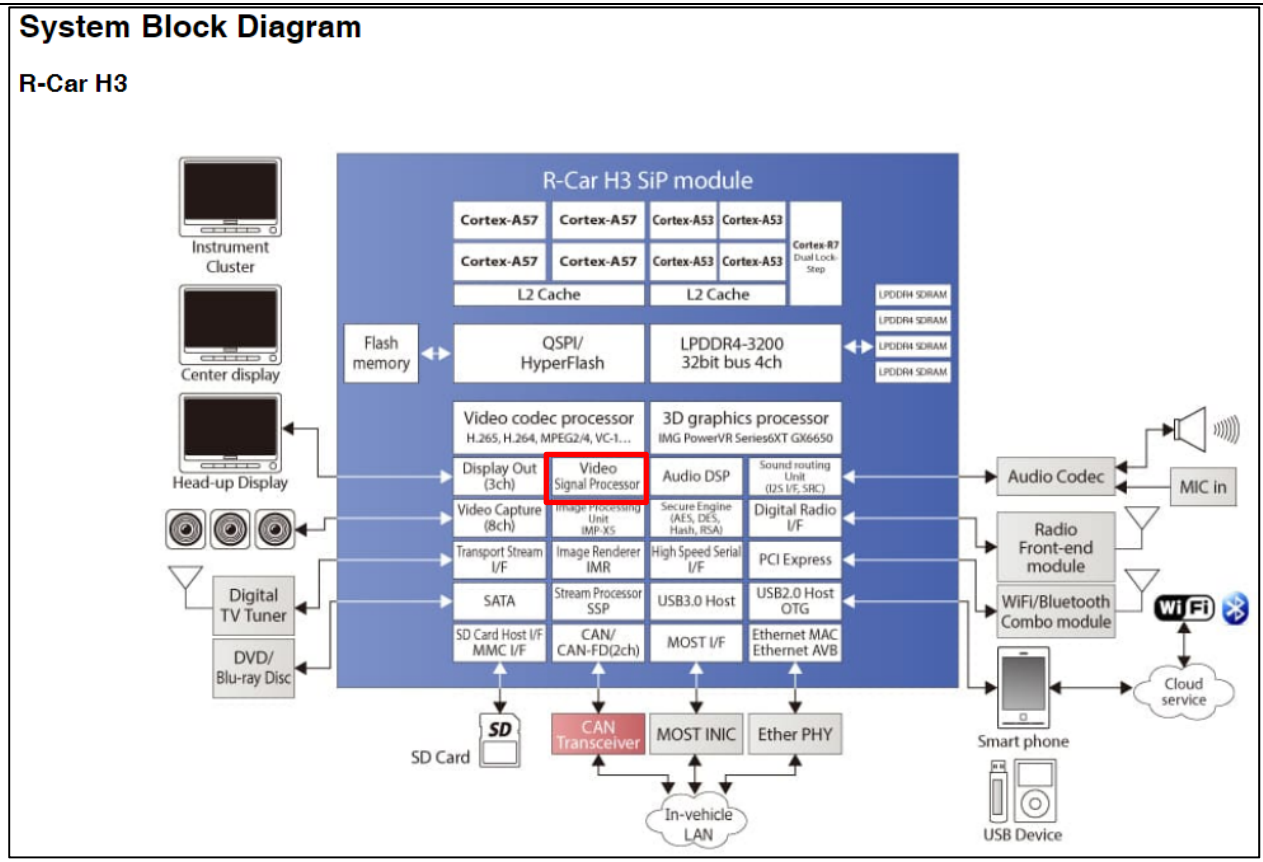


At least the Panasonic (AT1604) head unit, which is included in at least the Toyota Camry Navigation System (301378), includes a Renesas R-Car H2 SoC (highlighted in red).

	 Model No 86840-06011 Ref. No CN-SS87N0*XA Set No AT1604 DC 12V Negative Ground Panasonic Automotive Systems de Mexico S.A. de C.V. Serial No 112905



As explained in the R-Car Starter Kit H3/M3 Device Manual, the R-Car H3 includes a Video Signal Processor (VSP2) (red below), which supports image processing. Ex. 68 - Renesas R-Car H3/M3 Device Manual at 32-1.

	 Ex. 69 - Renesas R-Car H3 Specification at 3 (annotated)
a window controller for obtaining data that describes windows in which the graphics images are displayed, and for sorting the data in accordance with respective depths of the	The Accused Renesas Infotainment SoCs and head units and automobiles that incorporate the Accused Renesas Infotainment SoCs' system for processing graphics images comprise a window controller for obtaining data that describes windows in which the graphics images are displayed, and for sorting the data in accordance with respective depths of the windows. The R-Car Starter Kit H3/M3 Device Manual explains that the Data Path Router (DPR), which controls the data paths among RPFs, function modules, and WPFs, accesses data that describes windows in which the graphics images are displayed.

windows;

32.1.2.5 Data Path Router (DPR)

The DPR controls the data paths among RPFs, function modules, and WPFs. The DPR selects one of the images input from RPFs, outputs it to a function module (BRU, BRS, SRU, UDS, LUT, CLU, HST, HSI, HGO, HGT, SHP, UIF or ILV), and selects one of WPFs as the destination where the image data processed in the function module will be output. Before output to the WPF, the output from each function module can be input to another function module, which enables multiple image processing functions to be executed continuously without involving the external memory.

Ex. 68 – Renesas R-Car H3/M3 Device Manual at 32-15 (highlighted).

This includes the order of planes for blending, which can be sorted in accordance with the respective depth of the windows. Ex. 68 - Renesas R-Car H3/M3 Device Manual at 32-22 (highlighted).

Blending planes	Number of planes	Five planes selected from RPF0 to RPF4 and video processing function output, and virtual RPF; six planes in total
	Order of planes	The order of six planes selected from RPF0 to RPF4, virtual RPF, and video processing function output can be changed as desired.

Ex. 68 - Renesas R-Car H3/M3 Device Manual at 32-22 (highlighted).

When multiple source RPFs are used they are classified into master and sublayers by the window controller.

Note the following when specifying the source RPF.

(1) Each source RPF can be assigned to only one target WPFn; a single RPF cannot be assigned as the source RPF for multiple WPFs. For example, when setting VI6_WPF0_SRCRPF to 0x00000008 and VI6_WPF1_SRCRPF to 0x00000004 is attempted, the VSP2 will not operate correctly (these settings are prohibited) because RPF1 is assigned as both the master-layer source RPF for WPF0 and a sublayer source RPF for WPF1.

(2) When blending or ROP operation is applied to multiple images through the BRU or BRS, multiple source

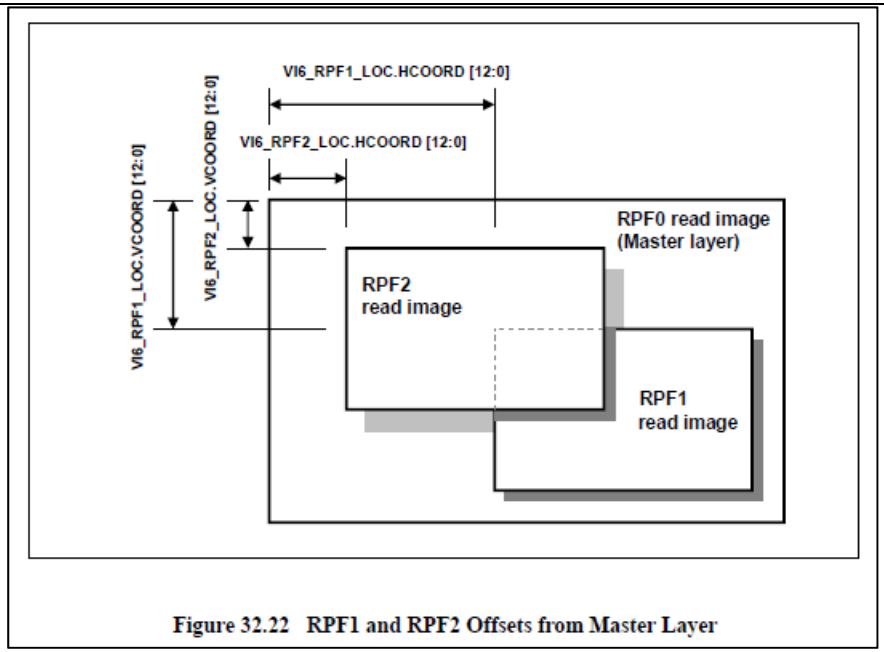
RPFs are necessary for one WPF. When multiple source RPFs are used, images should be classified into a master layer and sublayers; assign one of the source RPFs as the master-layer source RPF and other RPFs as sublayer source RPFs. Do not assign all RPFs as sublayer source RPFs (VI6_WPF1_SRCRPF = 0x00000015) or two or more RPFs as the master-layer source RPF (VI6_WPF0_SRCRPF = 0x0000025A) (such settings are prohibited).

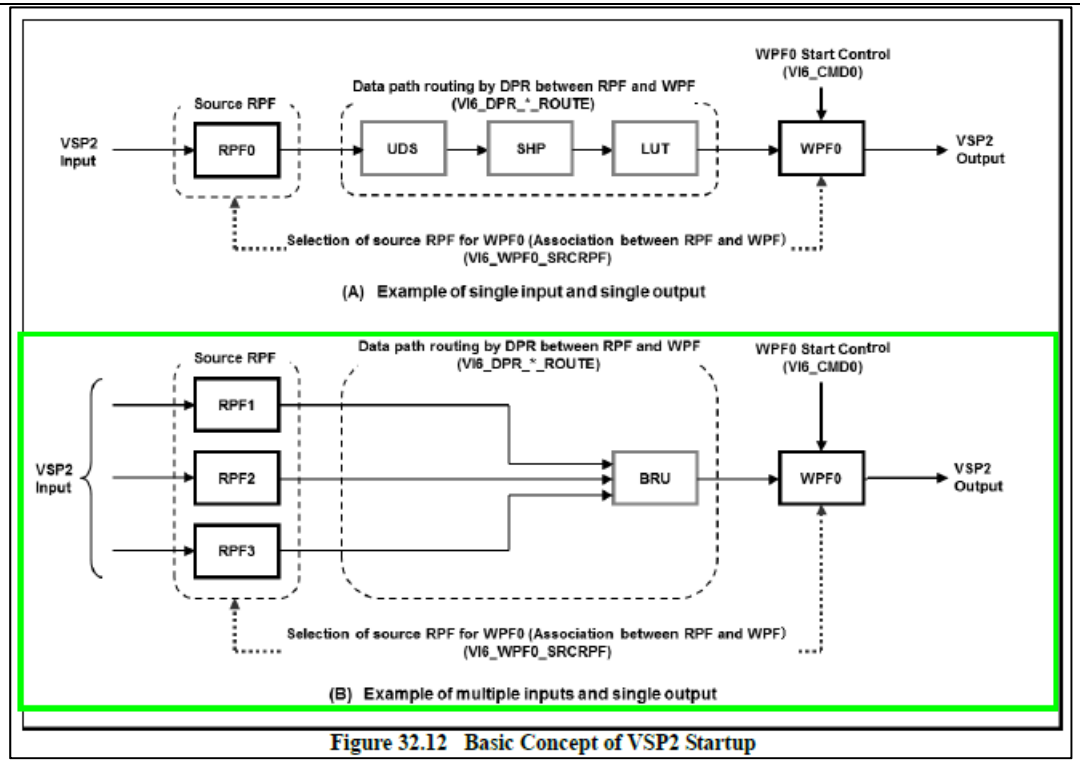
(3) When the BRU is not used, there should be only one source RPF for one WPF. In this case, the source RPF should be assigned as the master-layer source RPF.

Ex. 68 - Renesas R-Car H3/M3 Device Manual at 32-108-32-109 (highlighted).

9, 8	RPF4_ACT [1:0]	All 0	R/W	RPFn Start Enable (RPFn_ACT, n=0 to 4) These bits enable start of RPFn as the source RPF for the WPFn when the WPFn is started. When RPFn is not started by any of the WPF0 to WPF1, set the VI6_DPR_RPFn_ROUTE.RT_RPFn bits to D'63. 0: RPFn is not started. 1: RPFn is started as a sublayer source RPF for the WPFn. 2: RPFn is started as the master-layer source RPF for the WPFn. 3: Setting prohibited
7, 6	RPF3_ACT [1:0]	All 0	R/W	
5, 4	RPF2_ACT [1:0]	All 0	R/W	
3, 2	RPF1_ACT [1:0]	All 0	R/W	
1, 0	RPF0_ACT [1:0]	All 0	R/W	

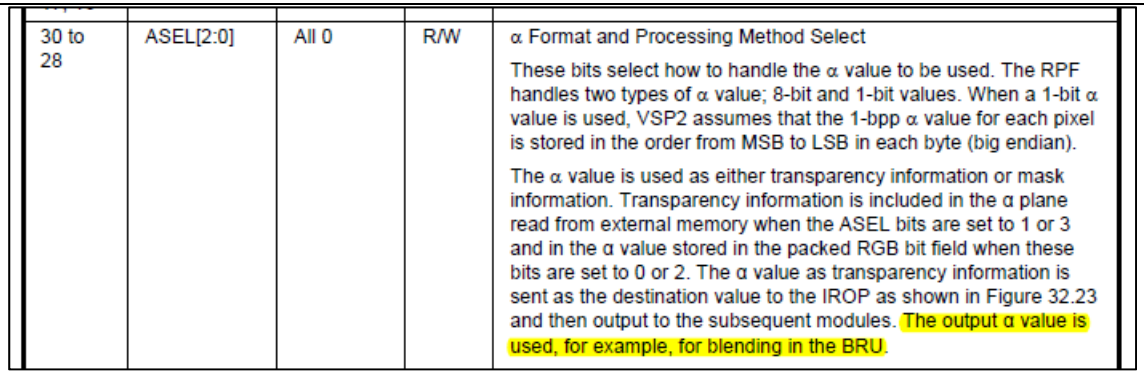
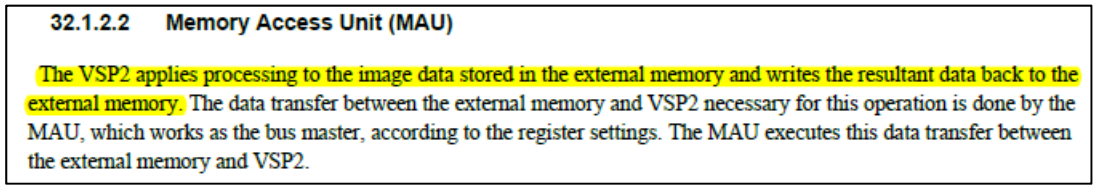
Ex. 68 - Renesas R-Car H3/M3 Device Manual at 32-108 (highlighted).

	 **Figure 32.22 RPF1 and RPF2 Offsets from Master Layer** Ex. 68 - Renesas R-Car H3/M3 Device Manual, Fig. 32.22, at 32-82.
a display engine for blending the graphics images using alpha values associated with the graphics images; and	The Accused Renesas Infotainment SoCs and head units and automobiles that incorporate the Accused Renesas Infotainment SoCs' system for processing graphics images comprises a display engine for blending the graphics images using alpha values associated with the graphics images. As is shown in the below Figure, the RPFn image planes are blended and then output.



Ex. 68 - Renesas R-Car H3/M3 Device Manual, Fig. 32.12, at 32-40 (annotated).

The R-Car Starter Kit H3/M3 Device Manual also explains that the RPFn α Plane Selection Control Registers are used for selecting the α Format and processing method, which is used for blending.

	 Ex. 68 - Renesas R-Car H3/M3 Device Manual at 32-83 (highlighted).
a memory for storing the graphics images,	The Accused Renesas Infotainment SoCs and head units and automobiles that incorporate the Accused Renesas Infotainment SoCs' system for processing graphics images comprises a memory for storing the graphics images. The R-Car Starter Kit H3/M3 Device Manual explains that "[t]he VSP2 applies processing to the image data stored in the external memory and writes the resultant data back to the external memory."  Ex. 68 - Renesas R-Car H3/M3 Device Manual at 32-14 (highlighted).
wherein the window controller transmits header packets to the display engine, each header packet containing at least a portion of the	The Accused Renesas Infotainment SoCs and head units and automobiles that incorporate the Accused Renesas Infotainment SoCs' window controller transmits header packets to the display engine, each header packet containing at least a portion of the data, said portion describing at least one of the windows. The window controller transmits header packets containing data describing the windows. For example, the input format, display location, and size of the image planes to be blended are defined by setting certain bits

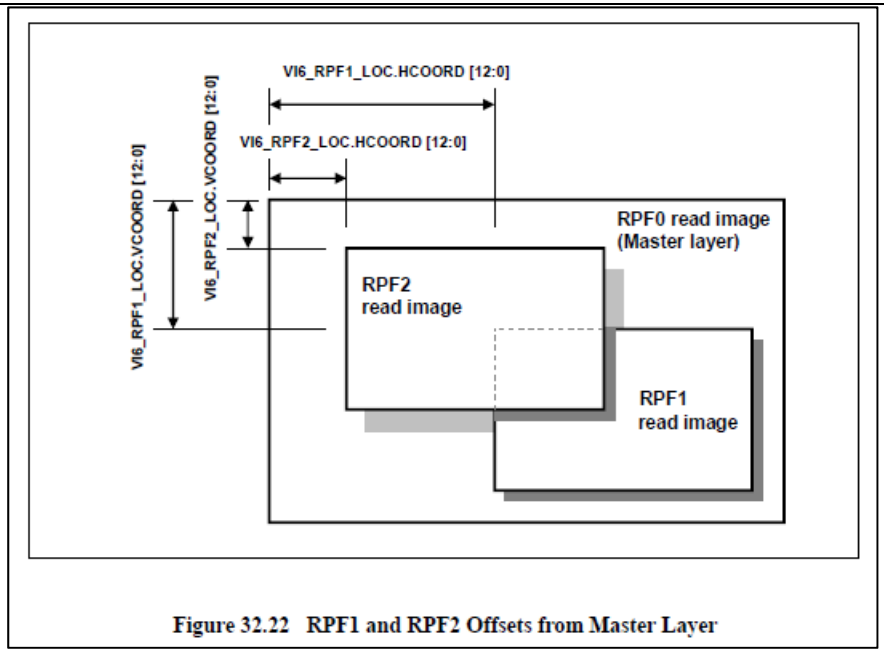
data, said portion describing at least one of the windows, and	in registers. **Table 32.4 VSP2 Register Configuration** Third Generation R-Car Series Products Register Name / Abbr. / R/W / Offset Address / Initial value / Access Size / R-CarH3 / R-Car M3 / | / | / | / | / |

RPFn Extended Read Size Registers	VI6_RPFn_SRC_ESIZE	R/W	H'0304 + H'0100*n	H'0000 0000	32	√	√					
RPFn Input Format Registers	VI6_RPFn_INFMT	R/W	H'0308 + H'0100*n	H'0000 0000	32	√	√					
RPFn Data Swapping Registers	VI6_RPFn_DSWAP	R/W	H'030c + H'0100*n	H'0000 0000	32	√	√					
RPFn Display Location Registers	VI6_RPFn_LOC	R/W	H'0310 + H'0100*n	H'0000 0000	32	√	√					
RPFn a Plane Selection Control Registers	VI6_RPFn_ALPH_SEL	R/W	H'0314 + H'0100*n	H'0000 0000	32	√	√					
RPFn Virtual Plane Color Information Registers	VI6_RPFn_VRTCOL_SET	R/W	H'0318 + H'0100*n	H'0000 0000	32	√	√					
RPFn Mask Control Registers	VI6_RPFn_MSKCTRL	R/W	H'031c + H'0100*n	H'0000 0000	32	√	√					
RPFn IROP-SRC Input Value Registers 0	VI6_RPFn_MSKSET0	R/W	H'0320 + H'0100*n	H'0000 0000	32	√	√					
RPFn IROP-SRC Input Value Registers 1	VI6_RPFn_MSKSET1	R/W	H'0324 + H'0100*n	H'0000 0000	32	√	√					
RPFn Color Keying Control Registers	VI6_RPFn_CKEY_CTRL	R/W	H'0328 + H'0100*n	H'0000 0000	32	√	√					
RPFn Color Keying Color Setting Registers-0	VI6_RPFn_CKEY_SET0	R/W	H'032c + H'0100*n	H'0000 0000	32	√	√					
RPFn Color Keying Color Setting Registers-1	VI6_RPFn_CKEY_SET1	R/W	H'0330 + H'0100*n	H'0000 0000	32	√	√					
RPFn Source Picture Memory Stride Setting Registers	VI6_RPFn_SRCM_PSTRIDE	R/W	H'0334 + H'0100*n	H'0000 0000	32	√	√					
RPFn Source α Memory Stride Setting Registers	VI6_RPFn_SRCM_ASTRIDE	R/W	H'0338 + H'0100*n	H'0000 0000	32	√	√					
RPFn Source Y/RGB Address Registers	VI6_RPFn_SRCM_ADDR_Y	R/W	H'033c + H'0100*n	H'0000 0000	32	√	√					
RPFn Source Chroma Address Registers 0	VI6_RPFn_SRCM_ADDR_C0	R/W	H'0340 + H'0100*n	H'0000 0000	32	√	√					
RPFn Source Chroma Address Registers 1	VI6_RPFn_SRCM_ADDR_C1	R/W	H'0344 + H'0100*n	H'0000 0000	32	√	√					
RPFn Source α Address Registers	VI6_RPFn_SRCM_ADDR_AI	R/W	H'0348 + H'0100*n	H'0000 0000	32	√	√					
RPFn Multiple Alpha Control	VI6_RPFn_MULT_ALPHA	R/W	H'036C+ H'0100*n	H'0000 0000	32	√	√					

Ex. 68 - Renesas R-Car H3/M3 Device Manual at 32-28 (highlighted).

Bit	Bit Name	Initial Value	R/W	Description
31 to 29, 15 to 13	–	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	HCOORD [12:0]	All 0	R/W	Horizontal Coordinate of Sublayer Display Location on Master Layer These bits specify the left-end location of the sublayer displayed by the RPFn and the subsequent module connected through the DPR. Specify the horizontal coordinate of the location in pixel units with the left-end pixel of the master layer set at coordinate 0. When the RPFn is the master layer, set these bits to 0. If the sublayer extends beyond the master layer according to the HCOORD setting, the extended section is cut off at the right end of the master layer. Even in this case, however, a bus transfer that is unnecessary for output image generation is executed since the whole sublayer data is read from the external memory. Appropriate coordinate setting is required so that the sublayer does not extend beyond the right end of the master layer. A value from 0 to 8189 can be specified.
12 to 0	VCOORD [12:0]	All 0	R/W	Vertical Coordinate of Sublayer Display Location on Master Layer These bits specify the top-end location of the sublayer displayed by the RPFn and the subsequent module connected through the DPR. Specify the vertical coordinate of the location in pixel units with the top-end pixel of the master layer set at coordinate 0. When the RPFn is the master layer, set these bits to 0. If the sublayer extends beyond the master layer according to the VCOORD setting, the extended section is cut off at the bottom end of the master layer. Even in this case, however, a bus transfer that is unnecessary for output image generation is executed since the whole sublayer data is read from the external memory. Appropriate coordinate setting is required so that the sublayer does not extend beyond the bottom end of the master layer. A value from 0 to 8189 can be specified.

Ex. 68 - Renesas R-Car H3/M3 Device Manual, Fig. 32.22, at 32-81 (highlighted).

	 **Figure 32.22 RPF1 and RPF2 Offsets from Master Layer** Ex. 68 - Renesas R-Car H3/M3 Device Manual, Fig. 32.22, at 32-82.
wherein the graphics images are transferred from the memory to the display engine responsive to said header packets.	The Accused Renesas Infotainment SoCs and head units and automobiles that incorporate the Accused Renesas Infotainment SoC transfers graphics images from the memory to the display engine responsive to said header packets. As explained in the R-Car Start Kit H3/M3 Device Manual, the RPF reads image data from the external memory. Ex. 68 - Renesas R-Car H3/M3 Device Manual at 32-14. Additionally, the setting of registers, which were set in accordance with the header packets, determines that the RPFn will be started and forms a data path between the RPF (entrance) and WPF (exit). Ex. 68 - Renesas R-Car H3/M3 Device Manual at 32-39.